ABSTRACT OF THE DISCLOSURE

An apparatus for detecting a predetermined pattern of bits in a data bitstream includes a series of detecting elements (2 –6), each detecting element in the series corresponding to a predetermined bit in the predetermined pattern. Each detecting element receives a data bit from the data bitstream (8), the corresponding predetermined bit in the predetermined pattern and an error signal from a previous detecting element in the series. The output of each detecting element is an error signal indicative of the number of mismatches between the data bit and the corresponding predetermined bit in the predetermined pattern, both in previous detecting elements in the series in previous clock cycles and in the current detecting element in the current clock cycle. The error signal of the final detecting element (6) of the series is coupled to a logic control element (18) for detecting that a maximum allowed level of mismatches has been detected.